Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 19 (cancelled)

Claim 20 (original): A method, comprising:

receiving on an integrated circuit from a switch fabric a first number of groups of switch cells, each switch cell having a switch header and a data payload, each of the groups being destined for one of a second number of output ports of the integrated circuit, the first number being greater than the second number;

storing each of the data payloads of the first number of groups into a corresponding one of a plurality of buffers;

retrieving from the plurality of buffers the data payloads of one of the groups of switch cells destined for each of the output ports, and outputting from the integrated circuit the data payloads retrieved such that a reassembled packet is transmitted onto a fiber optic cable for each of the groups of switch cells retrieved, the reassembled packet of a group comprising the data payloads of the switch cells of the group, the data payloads of no more than one group for each output port being output at any one time; and

maintaining a reassembly context for each group of data payloads being retrieved from the plurality of buffers, each group of data payloads being retrieved being destined for a different one of the output ports such that the integrated circuit maintains no more than one reassembly context per output port.

Claim 21 (original): The method of Claim 20, wherein the output ports are logical output ports associated with a single physical output port.

Claim 22 (original): The method of Claim 20, wherein the data payloads of one of the groups of switch cells are AAL5 adaptation layer cells, one of the AAL5 adaptation layer cells including a trailer, the trailer including a CRC, the integrated circuit not checking the CRC in the trailer

prior to storing the data payloads of the group into the plurality of buffers.

Claims 23 – 33 (cancelled)

Claim 34 (original): The method of Claim 20, wherein the integrated circuit includes a reassembly block, and wherein each reassembly context includes a running byte count value, the running byte count value of the reassembly context for an output port being updated as each successive data payload of the switch cells of a group destined for the output port passes into the reassembly block, the reassembly block using the running byte count value to remove padding from a last of the data payloads, the last of the data payloads being marked by an EOP bit.

Claim 35 (original): The method of Claim 20, wherein each reassembly context includes a running byte count value and a partial CRC value.

Claim 36 (original): A method comprising:

outputting a plurality of chunks of information from an integrated circuit and storing the plurality of chunks into a plurality of buffers in a payload memory external to the integrated circuit;

retrieving the plurality of chunks from the payload memory and processing those chunks sequentially through a reassembly block on the integrated circuit;

maintaining a running byte count value which is updated by the reassembly block as each of the chunks passes into the reassembly block; and

using the running byte count value to reassemble the chunks such that the chunks form a packet, wherein the integrated circuit is usable in an ingress mode and in an egress mode, wherein in the ingress mode the packet is transferred to a switch fabric, and wherein in the egress mode the packet is transmitted onto a network.

Claim 37 (original): The method of Claim 36, wherein the packet is output from the integrated circuit onto an SPI-4 bus, wherein the SPI-4 bus is coupled to the switch fabric if the integrated circuit is operating in the ingress mode, and wherein the SPI-4 bus is coupled to a framer if the

integrated circuit is operating in the egress mode.

Claim 38 (original): The method of Claim 36, wherein the chunks are processed through the reassembly block sequentially such that a part of the packet is transferred out of the reassembly block before one of the chunks has been retrieved from the payload memory.

Claim 39 (original): An integrated circuit having one or more active output ports, comprising:

a memory manager that stores chunks of information into buffers in a payload memory, all the buffers being of equal size, some of the chunks including cell information, others of the chunks including packet information;

a reassembly engine that receives said chunks from the memory manager and that performs only one reassembly process at any given time for each active output port, the reassembly engine maintaining substantially no more than one reassembly context for each active output port, a reassembly context including a partial byte count and a partial CRC; and

a mode control register, wherein placing first configuration information in the mode control register causes the integrated circuit to operate in an ingress mode, and wherein placing second configuration information in the mode control register causes the integrated circuit to operate in an egress mode.

Claim 40 (original): The integrated circuit of Claim 39, wherein the reassembly engine comprises:

a port calendar;

a data memory comprising a plurality of buffers;

an enqueue state machine for queuing said chunks into said data memory on a per output port basis; and

a dequeue state machine for dequeuing said chunks from said data memory in accordance with an output port identifier received from the port calendar.

Claim 41 (cancelled)

Claim 42 (currently amended): ~~The integrated circuit of Claim 41,~~ An integrated circuit having one or more active output ports, comprising:

a memory manager that stores chunks of information into buffers in a payload memory, all the buffers being of equal size, some of the chunks including cell information, others of the chunks including packet information; and

reassembly means for receiving said chunks from the memory manager and for performing one reassembly process per active output port such that substantially no more than one reassembly context is maintained for each active output port,

wherein the memory manager stores said chunks in the payload memory in per flow queues, and wherein the reassembly means stores said chunks in per port queues.

Claim 43 (currently amended): ~~The integrated circuit of Claim 41, further comprising:~~ An integrated circuit having one or more active output ports, comprising:

a memory manager that stores chunks of information into buffers in a payload memory, all the buffers being of equal size, some of the chunks including cell information, others of the chunks including packet information;

reassembly means for receiving said chunks from the memory manager and for performing one reassembly process per active output port such that substantially no more than one reassembly context is maintained for each active output port; and

a mode control register that stores configuration information, wherein the integrated circuit is configured in an ingress mode if first configuration information is stored in the mode control register, and wherein the integrated circuit is configured in an egress mode if second configuration information is stored in the mode control register.

Claim 44 (currently amended): The integrated circuit of Claim ~~41~~ 42, wherein the reassembly means processes a chunk in one of a plurality of ways as determined by type information, the type information for a chunk being passed from the memory manager to the reassembly means along with the chunk.

Claim 45 (new): The integrated circuit of Claim 43, wherein the reassembly means

processes a chunk in one of a plurality of ways as determined by type information, the type information for a chunk being passed from the memory manager to the reassembly means along with the chunk.